This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1(currently amended). A chip diode for surface mounting, comprising:

a first type semiconductor having a predetermined depth formed on a first surface of a semiconductor wafer by diffusion;

a second type semiconductor having a predetermined depth formed on a second surface of [[a]] the semiconductor wafer by diffusion wherein the second type semiconductor is different from the first type semiconductor and the second surface is opposite the first surface;

a plurality of diodes formed on each of the first and the second surfaces of the semiconductor wafer;

a plurality of first insulation layers formed on the diodes at the first surface of the semiconductor wafer for dividing the semiconductor wafer into two separated and insulated portions;

a plurality of first conductive metal layers coated on a central portion of the semiconductor wafer as a first conductive terminal for soldering; and

a plurality of second conductive metal layers coated on an edge of the semiconductor wafer and extended to sides of the second type semiconductor on the second surface of the semiconductor wafer to be in communication therewith as a second conductive terminal for soldering.

2(original). The chip diode of claim 1, wherein each of the first and the second conductive metal layers is formed by chemically plating at least one layer of conductive metal on a first surface of the diodes corresponding to a central portion of the semiconductor wafer.

3(currently amended). The chip diode of claim 2, further comprising:

a plurality of parallel, spaced first grooves and second grooves formed on the first type semiconductor at the first surface of the diodes along X and Y axes respectively by etching, each of the first grooves and the second grooves being penetrated through the first type semiconductor into the second type semiconductor; and containing a plurality of the first insulation layers in the first and the second grooves formed by sintering, the first insulation layers being adapted to separate and insulate the first type semiconductor from the second type semiconductor at both sides.

4(original). The chip diode of claim 3, wherein the first insulation layers are glass insulation layers formed by sintering glass plasma.

5(original). The chip diode of claim 3, further comprising at least one trough formed on the second surface type semiconductor at a second surface of the diodes along X axis by etching wherein a bottom of each trough is spaced from that of each of the first grooves and the second grooves by a predetermined distance and a width of each trough along X axis direction is approximately equal to a distance between two adjacent second grooves.

6(original). The chip diode of claim 5, wherein each of the second conductive metal layers comprises:

a first conductive metal stratum sintered in the troughs;

a second conductive metal stratum sintered in at least one side of the diodes and extended in sides of the first and the second type semiconductors to be in communication with the first conductive metal stratum; and

a third conductive metal stratum formed by chemically plating at least one layer of conductive metal on the first surface of the diodes corresponding to edges of the first and the second type semiconductors and the second conductive metal stratum.

7(original). The chip diode of claim 6, further comprising a plurality of second insulation layers formed on the first conductive metal stratum by sintering.

8(original). The chip diode of claim 7, wherein the second insulation layers are glass insulation layers formed by sintering glass plasma.